Q.P. Code: 20CS0504 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Regular & Supplementary Examinations March-2023

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to CSE,CSM,CIC,CAD,CCC & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units 5 x 12 = 60 Marks)

		UNIT-I			
1	a	Describe the Basic Operational Concepts of computer with neat diagram.	CO1	L2	8M
	b	What are the Purpose of PC, IR and General-Purpose Registers?	CO1	L1	4M
		OR			
2	a	Identify and explain various Phases of instruction cycle.	CO1	L3	10M
	b	List the Classification of Computer Instructions.	CO2	L2	2M
		UNIT-II			
3		Illustrate the steps in Booth multiplication flow chart. Show the step by step signed multiplication of (-7) and (-11) using Booth algorithm.	CO3	L6	12M
		OR			
4		Discuss the Multiplication algorithm with Shift and add method with suitable flowchart. Multiply the binary numbers (01011) and (01101) Using Shift and add method.	CO3	L3	12M
		UNIT-III			
5	a	Discuss the any four Arithmetic Micro Operations.	CO3	L3	6M
	b	Draw and explain four bit parallel adder circuit.	CO3	L2	6M
		OR			
6	a	Describe the Micro Programmed Control with a neat sketch.	CO6	L2	6M
	b	What is micro programmed control? List the advantages.	CO6	L2	6M
		UNIT-IV			
7	a	Compare various types of Auxiliary memories.	CO2	L2	6M
	b	Define track and sector. Analyze the importance of auxiliary memory.	CO3	L3	6M
		OR			
8	a	Classify the ROM memories.	CO3	L3	2M
	b	Explain different ROM memories.	CO4	L2	10M
		UNIT-V			
9	a	What are the sub operations performed in arithmetic pipelining?	CO6	L2	4M
	b	Sketch the flowchart for floating point multiplication in arithmetic pipeline.	CO5	L3	6M
	c	Calculate the delay time in an equivalent non-pipeline floating point adder subtractor, when t1=60ns,t2=70ns,t3=100ns,t4=80ns,tr=10ns.	CO5	L3	2M
		OR			
10	a	Define interconnection network, bandwidth and effective throughput.	CO6	L2	6M
	b	Explain the bus in interconnection network.	CO6	L2	6M

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